ALMA Memo No. 462

Effects of Radiation on the ALMA Correlator

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Abstract

This memo looks specifically at the effects of cosmic ray radiation at the high ALMA site on the ALMA Correlator. The most vulnerable components of the Correlator are the 17,066 Xilinx Field Programmable Gate Arrays (FPGA). The primary risk is that radiation would cause bits in the downloaded configuration to change. This could change the FPGA's functionality, until reloaded. The most practical remedy is to periodically download the Xilinx personalities. This would reverse the effects of a rare error induced by radiation.

1. Introduction

ALMA Memo No. 446 "Levels of radiation exposure near AOS and OSF" brought up concerns about the effects of radiation on integrated circuits at the high altitude ALMA site. The ALMA High Altitude site is subject to increased radiation from cosmic rays, due to less atmospheric shielding than at sea level.

As altitude increases, there is an increase in true cosmic rays (relativistic, ionized, relative heavy ions) since there is less atmosphere between the source (galactic deep space) and the subject. These are the same ions (cosmic rays) encountered in orbit. However, at the altitude of the AOS, they are a minor consideration. The major radiation flux is from neutrons, which are a problem only because their collision products include charged particles such as alphas. This can cause a Single Event Upset (SEU).

A more serious radiation event is a Single Event Latchup (SEL). At this altitude SEL is not a concern. SEL is caused by basically shorting Vdd to Vss. When an energetic particle penetrates the substrate and active regions, it leaves an ionization trail of hole-electron pairs. The recombination of the electron-hole pairs generates recombination current. That current can activate the parasitic bipolars and create a short circuit between Vdd and Vss. This may or may not be destructive based on many factors like layout and amount of current available.

2. The Effects of Radiation on ALMA1s vs. Xilinx FPGAs

The initial concern was for the 32,768 ALMA1 Correlator Chips that will be part of the Correlator. That concern spread to include the 17,066 Xilinx FPGAs. Lou Morales of Innotech, which manufactures the ALMA1 chips, provided input information, along with Jason Moore of Xilinx.

A. Device Technology

The ALMA1 would tend to be less susceptible than the Xilinx due to the technology difference. The ALMA1 uses 0.25 micron technology, versus 0.18 micron for the Xilinx FPGAs. For smaller device features, the effect of a neutron would be more pronounced.

B. Device Operation Voltage

The ALMA1s will be operated at 1.8 Volts, instead of the nominal process voltage of 2.5 Volts. This lowers power dissipation. The Xilinx Virtex-E FPGAs will be run at their nominal voltage of 1.8 Volts. The use of relatively low voltage on the ALMA1's 0.25 micron technology raises its SEU susceptibility. In fact, low voltage operation of 0.25 micron technology might result in worse susceptibility than nominal voltage operation of 0.18 micron technology.

The increase of SEU susceptibility in chips, like commercial SRAMs, with lowered operating voltage is well documented.

C. Quantity of Devices

There will be 32,768 ALMA1 chips. There will be 17,066 Xilinx FPGAs. These numbers favor a SEU event occurring more often in an ALMA1.

D. Effect a SEU can have on ALMA1 Data Integrity

Each ALMA1 has a 128-bit program register that determines the chips functionality.
An SEU toggling one of these flip-flops would change the chips functionality. There are 176,128 flip-flops in the 4096 lags of an ALMA1 chip. This is 1376 times the number of flip-flops in the program registers. So most likely, an SEU would occur in a lag flip-flop. This would affect the data integrity. However, the corruption would be of a single lag, in a single 16 ms integration.

E. ALMA1 Data Integrity vs. Xilinx FPGA Data Integrity

The table in the next section shows that the smallest Xilinx chip used has 630,048 configuration flip-flops. This is about four times the number of flip-flops in an ALMA1 chip. An SEU in a configuration flip-flop could alter the functionality of the Xilinx

FPGA. Thus Xilinx FPGAs are much more at risk from SEUs. The remainder of the discussion focuses on the Xilinx FPGAs.

3. The Effects of Radiation on Xilinx FPGAs

A. General Information

Xilinx has done extensive research into these effects.
Refer to The Xilinx Application note:

http://www.xilinx.com/xapp/xapp181.pdf
“SEU Mitigation Design Techniques for the XQR4000XL”

This Application Note describes:
“As an IC is bombarded with radiation particles, a temporary logic state change can occur within the IC. This phenomenon is known as Single Event Upset (SEU). This effect can manifest as a transient upset which can last a few nanoseconds, or as a static upset which changes the stored charge of a static cell. For simple gates, a transient glitch in the logic is usually not an issue. When an SEU occurs within the latch that makes up a flip-flop or memory cell, however, the effects on functionality are often problematical. Since a flip-flop is a memory device, the flip-flop can change state and remain in that state until the next occurring clock or reset. In this condition the flip-flop is said to have been “upset” (i.e., its state has changed independently of circuit operation). Likewise the configuration latches, which define the user’s design functionality, can be also susceptible to static upsets.”

Thus, the configuration memory cells are just as susceptible to SEUs as are the design-specified flip-flops. There are many times the number of configuration memory cells as there are design-specified cells.   These configuration latches determine the functionality of the FPGA.   The actual number of design-specified cells used depend on the Xilinx programmed functionality.

B. Xilinx Risks in the ALMA Correlator

An SEU affecting the data stream in an ALMA1 chip or a Xilinx chip would change that data, but the effect would be transient. An SEU in the configuration of a Xilinx could be more severe. If the Xilinx’s configuration is changed, it may not function in the manner intended. To correct the configuration, the FPGA would have to be reprogrammed.
For the ALMA Correlator, reprogramming the Xilinxs requires ceasing operation for the duration of the reprogramming.

C. Quantitative Analysis of Xilinx Risks

The Xilinx population of the full, Four Quadrant Correlator, sorted by chip type will be:

Xilinx Type	Gates/Chip	Chips in Correlator	# of Configuration Bits / Chip
XCV50E	71,693	11000	630,048
XCV100E	128,236	1600	863,840
XCV200E	306,393	266	1,442,016
XCV400E	569,952	4200	2,693,440
	Total	17,066	

The risk of an SEU is proportionally higher in a Xilinx FPGA with more gates and configuration bits. The large number of Xilinx chips makes SEU events, even if rare, still a concern.

Jason Moore and Joe Fabula of Xilinx provided some custom analysis of the situation of Xilinx chips in the ALMA Correlator.

MTBF (Mean Time Between Failure) is the average time between there being a SEU event (that cause a logic failure) in any Xilinx chip in the ALMA Correlator.

Based on their analysis, for an altitude of 16,500 feet, and latitude of -30 degrees, the MTBF would be 312 hours. That is, on average, every 312 hours, there would be flip flop toggled due to radiation, in the ALMA Correlator Xilinx chips.

At sea level the MTBF would be 22 times as long (22*312=6864 hours), due to the decrease in neutron flux .

4. Methods of Reducing the Effects of Radiation

A. Implement the Enhanced Filter Card with Custom ASICs

The XCV400E are the most prone to SEU events of the Xilinx chips. That is because the XCV400E Xilinx has the most configuration flip-flops. The XCV400E FPGAs are exclusively used on the filter cards. The filter cards contain a total of 4200 XCV400E Xilinx chips.

An alternate version of the filter card is being considered to give enhanced capabilities. This enhanced filter card might use custom ASICs instead of the XCV400E Xilinx chips. Joe Fabula recalculated the MTBF of the Xilinxs in the ALMA Correlator without the XCV400Es to be 716 hours. The MTBF was 312 hours with the XCV400Es.

Note this does not take into account any SEU failures in the ASICs which replace the Xilinx FPGAs. However, SEUs in the ASICs would probably be in the data stream, instead of configuration flip-flops. These transient events would be less damaging.

B. Radiation Hardened Chips

Xilinx manufactures the QPRO line which is radiation hardened. However this is not a cost effective alternative, since the chips are very expensive. Also they are not pin compatible with the current designs, so a redesign would be needed.

C. Shielding

Jason Moore of Xilinx said that additional shielding is not an effective option. The SEUs are mainly caused by neutrons. The neutrons would easily go through twenty feet of concrete.

D. Detection of SEU Induced Errors

If an error could be detected, then it could be corrected or flagged. A periodic system test could be one method of detecting errors.

Loading Xilinx personalities with redundant, parallel paths could provide SEU detection. If two redundant functions yield different answers to the same data, an error could be assumed. If there are three redundant paths, there could be a voting, and the majority could be used to ensure correct data.

If there are portions of the Correlator not being used, that portion could be used as a parallel path. Both paths yielding the same result would verify proper operation. Three or more paths could be used for a voting situation.

E. Scrubbing

Given that SEU events will occasionally occur, it is desirable to not let the effects stay around too long. Reloading the Xilinx personalities will reset any reconfiguring that has occurred. This is called Scrubbing. Xilinx gave a rule of thumb of reloading the Xilinx FPGAs at a rate of one tenth the MTBF. For the MTBF of 312 hours, that would be every 31 hours.

It is proposed that, at least daily, the Correlator will be brought off line, and put through a complete system test. This would test for any failures that had occurred since the last system test. This sort of test would also be desirable for detecting other system faults, such as failed chips. Part of this test would include a complete reload of the Xilinx personalities. The complete test should take less than five minutes. The Xilinx reload should take less than one minute. This would fulfill the Scrubbing requirement.

Doing a system test before and after reloading the Xilinx personalities could detect possible radiation effects.

There are methodologies for continually reloading the Xilinx personalities while the chips are in use. However, that functionality has not been designed into the hardware of the current Correlator.

5. Conclusions

The ALMA Correlator will be subject to the effects of radiation at the ALMA High site. The most vulnerable area is the storage of the Xilinx configurations in each Xilinx FPGA. There is a MTBF of 312 hours for all the Xilinx FPGAs in the Correlator. If the Enhanced Filter Cards with Custom ASICs are chosen, that will eliminate the largest FPGAs, bringing the Xilinx MTBF to 716 hours (29.8 days).

Statistically, radiation would induce an error in one chip in the Correlator once a month. This is not an important source of error.

The most probable method of control could be to reload the Xilinx FPGAs in the entire Correlator at least once a day, probably during a scheduled system test. At this time, the ALMA1 Program words could also be reloaded, in case they were corrupted. This would minimize the occasional loss of data due to radiation.