ALMA Memo No. 426

4-GSample/s, 2-bit SiGe Digitizers for the *ALMA* Project. Paper II

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Abstract

We report on the design details and first dynamic tests of high speed analog-to-digital converters (ADCs) with characteristics approaching those desired for the ALMA project. A conventional flash ADC architecture has been adopted with monolithic ADCs implemented in BiCMOS 0.35 µm and 0.25 µm SiGe (Silicon-Germanium) processes. We concentrate here on our 2-bit, 0.35 µm designs and test results, while details on our 3-bit designs and 0.25 µm SiGe technology will be given in another paper. The main features of these 2-bit ADCs are a 4 GHz clock rate, 3 quantization levels, and an input bandwidth from 2 GHz up to 4 GHz. The two chips tested in this work dissipate 650 and 975 mW under 2.5 V supply; the die areas are 5.4 mm^2 and 6.5 mm^2, respectively.

1. Introduction

To enhance the sensitivity of radio interferometers and of single-dish radio antennas it is essential to process broad bandwidths (> 0.5 to 1 GHz is required in many projects) and thus to design broadband analog-to-digital converters (ADCs or digitizers) clocked at high speeds. In this paper we present the main features of high speed monolithic digitizers that we have implemented in BiCMOS 0.35 µm SiGe processes for radio astronomy applications and, in particular, for the ALMA project. These digitizers work with a 2-4 GHz input bandwidth and deliver 2 bits at a rate of 4 gigasamples per second (Gsps). Our 3-bit designs (the ALMA goal) use 0.25 µm SiGe processes and will be presented in a future paper. The approach followed to design and test our high speed ADCs has been described in [1, Paper I].

A review of state of the art commercial samplers with conversion rates above 1 Gsps shows that the ADCs required for ALMA doe not exist off the shelf. Some commercial products reach 1-2 Gsps and in one case 4 Gsps is reported; however, no device has an input bandwidth up to 4 GHz. Moreover, several commercial products offer more bits than actually required for radio astronomy and their high power dissipation does not make them much attractive for the ALMA project.

The III-V (GaAs or InP) technology is often brought into play to operate at such high frequencies [2]. Usually, classical technologies based on Silicon are not fast enough to work at sample rates beyond 1-2 Gsps [3, 4]. Nowadays, the technologies based on SiGe heterojunction bipolar transistors (HBTs) are competitive with III-V technologies in the range 1-10 GHz. The technology adopted here is based on the SiGe BiCMOS 0.35 µm and 0.25 µm processes from STMicroelectronics. A first 1-bit digitizer design was made with the HCMOS7 0.25 µm process. However, this technology is not fast enough to achieve 2-4 GHz bandpass sampling. SiGe bipolar transistors have a transition frequency equal to 45 GHz for 0.35 µm process and 75 GHz for 0.25 µm process. These processes allow us to achieve wide bandwidth amplification and to design high speed comparator cells without excessive amount of power.

In Section 2, we briefly recall the ALMA digitizer top level requirements. In Section 3, we describe the data conversion structure used for the ALMA ADCs. Section 4 describes two different circuit designs. Results of first experimental tests are briefly discussed in Section 5.

2. ALMA Digitizer Requirements

The ADC input bandwidth for the ALMA project is from 2 GHz up to 4 GHz. The response of this circuit must be linear and the ripple over 2-4 GHz should not exceed ±0.5 dB. It must be matched to 50 Ω. The top level performances required for the ALMA digitizers have been discussed in ALMA Memo 410 [1]. They are summarized in Table 1 below.

Table 1. ALMA digitizer performance requirements

Input Bandwidth	2-4 GHz
Sample Clock	4 GHz (250ps)
Bit resolution	3 bits and 2 bits
Quantization levels	8 and 3
Aperture time	< 50 ps
Aperture jitter	~2 ps
Indecision level	~ a few mV
Power dissipation	< 2 W

The power supply is limited here to 2.5 V while most ADCs are designed and optimized for higher voltages. Usually, with GaAs technologies, the power supply is 5 V, while with Si or SiGe technologies it does not exceed 3 V [5]. Hence, our digitizer design must be optimized for low voltage, low consumption and wide bandwidth.

3. Analog Data Converter Architecture

Complex architectures resulting from sigma-delta and successive approximation are not appropriate for high speed ADCs because of their low speed. Our designs for the ALMA project use a straightforward fully parallel or flash architecture. Each period of the clock provides one converted data which is the fastest way to convert an analog signal into a digital one. Flash ADCs using simultaneously 2^n-1 comparators for an n-bit circuit are thus well suited to high speed conversion. However, the main drawback of this architecture is that it is not suited for high resolution (> 4-8 bits) each additional bit resolution increasing exponentially the size and the consumption of the ADC core circuitry. In most radio astronomy applications a resolution of 2 bits is sufficient (see also universal figure of merit of digitizers in [1]).

An ADC can be easily implemented in an integrated circuit by addition of comparator blocks provided that one pays attention to signal paths and mismatching delay times. In the ALMA case the low number of bits allows us to keep the chip complexity and the power consumption at a rather low level. The chip layout requires to minimize the aperture time error due to routing path mismatches between the input adapter amplifier and the comparators as well as between the clock distributor and the comparators. Under 2.5 V voltage supply one cannot stack more than 2 or 3 transistors. Therefore, typical comparator and latch structures must be updated to deal with this weak power supply. We have chosen for our first designs a symmetrical supply voltage of ±1.25 V.

4. Designs of 2-bit ADCs

4.1 0.35 µm and 0.25 µm SiGe processes

We have designed three different 2-bit ADCs (see Table 3 in [1]), two in BiCMOS6G (0.35 µm) technology and one in BiCMOS7 (0.25 µm) technology. A first design layout was sent to foundry in February 2001; this design was made to validate the BiCMOs SiGe technology chosen by us and to make us accustomed with the design tools. The second 2-bit ADC design is more 'robust' in terms of technological and thermal dispersions and was sent to foundry in August 2001. It contains a new input adapter amplifier for better broadband matching, and a new clock amplifier; thereby a new package was required. The 2-bit ADC design of December 2001 used the latest BiCMOS technology from STMicroelectronics and new design kit tools. The latter design is similar to the design of August 2001 and was sent to foundry to evaluate the performances of the newer SiGe7 technology (0.25 µm process) which we use for our 3-bit designs. This 2-bit, SiGe7 chip is being packaged and should be available soon.

Our 2-bit monolithic chips integrate an input adapter amplifier, comparators with associated master-slave latches, a clock generator, biasing cells and output buffers. The input signal, a Gaussian statistics 'white noise' signal over 2 GHz bandwidth, is amplified and compared with two reference thresholds. Figure 1 shows the complete 2-bit digitizer circuit configuration.

Fig. 1. Two-bit digitizer circuit configuration

4.2 February 2001 design (0.35 µm process)

A. Input adapter amplifier

The main goals of the input adapter amplifier (Fig. 2) are to buffer and convert the input asymmetrical signal into a differential one for the sampling process.

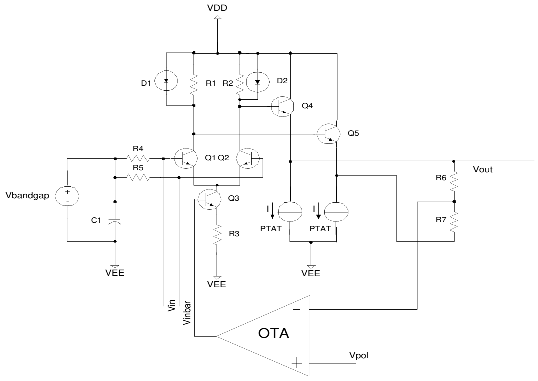

Fig. 2. Schematic of the input adapter amplifier

The signal path is differential through the amplifier, comparators, latches and output buffers in order to reduce the effects of clock and substrate noise. The input stage is a differential amplifier whose current source is driven by an OTA. This common mode feedback loop allows us to lock the mean value of the amplifier output voltage to –150 mV which is the central threshold for the comparators. The input stage is biased by a bandgap voltage generator to be less sensitive to temperature and power supply variations. Broadband impedance matching is accomplished by internal poly-silicon 50 Ω resistors.

The output stage is made up of two buffers biased by a 'Proportional To Absolute Temperature' (PTAT) current source. Diodes D_1 and D_2 are mandatory to avoid saturation of the input amplifier by the input voltage due to Gaussian statistics peaks. In fact, the amplifier does not have to spend time to eliminate charges stored in saturated NPN transistors. Fig . 3 shows the schematic of the OTA amplifier.

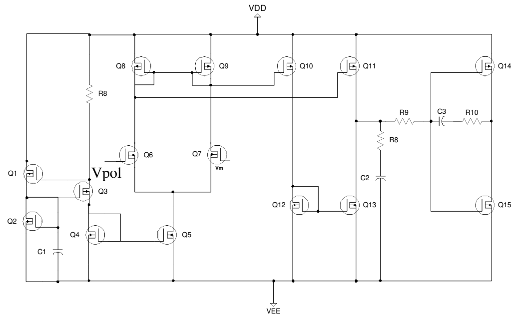

Fig. 3. Schematic of the OTA amplifier

B. Comparator/Sampler

The sampling function is performed in the comparator cells, which include a comparator and two latches in a master-slave configuration clocked at 4 GHz. This structure suppresses metastability state by providing more amplification of the input signal and better conversion speed by holding a stable comparison result. The comparator shown in Fig. 4 includes two amplifier cells in order to minimize the hysteresis. The first one subtracts the input signal and the second one amplifies this difference. The comparator hysteresis must be kept as small as possible because it determines the digitizer indecision level; our goal is of the order of 1 millivolt. Should the value of the comparator hysteresis be high, the amplifier gain and the comparator threshold voltages have to be increased in order to keep the ratio between the comparator window and the indecision level constant.

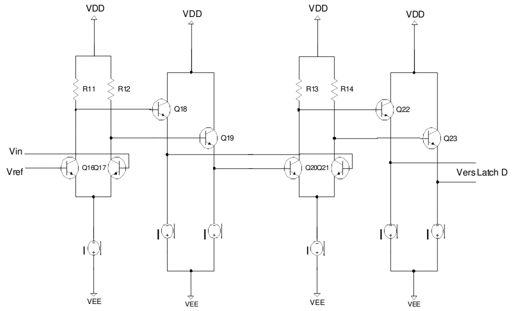

Fig. 4. Schematic of the comparator

This comparator is followed by two latches achieving the sampling and storing process with master/slave configuration. The D-latch is loaded by a differential amplifier to add gain, in order to minimize the indecision region and to adapt the mean level of the output buffers (Fig. 5). The latch sampler circuit alternates between the sampling mode and the latching mode by switching on CK and CKbar signals.

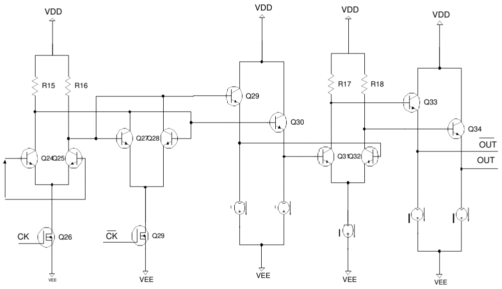

Fig. 5. Schematic of D-latch

Because of reduced power supply, it is not possible to stack more than two NPN transistors without one of them working in its saturated region. Thus, classical latch structures have to be modified. The clock is applied on the current source to reduce the number of stacked transistors. The NMOS transistor driven by the clock is a current source during one half-period and an open switch during the remaining half period.

C. Clock distributor circuit

The clock signal applied to the die is a 0 dBm 4 GHz sinusoidal waveform with not sharp enough rise and fall edges. Thus, we need to transform the sinusoidal waveform into a square signal. The clock amplifier inputs must be matched to 50 Ω. Bypass capacitances are integrated and made of metal-metal capacitances. The clock distributor circuit (Fig. 6) is made up of three differential amplifiers which generate CK signal and Ckbar signal. This circuit is loaded by a buffer which controls the high level CK and Ckbar signal voltages.

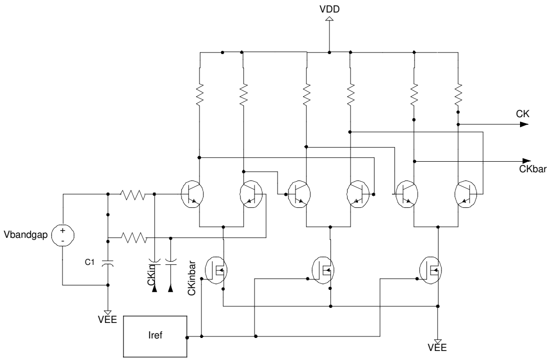

Fig. 6. Schematic of clock distributor circuit

D. Output coding

An encoding system is not necessary for a 2-bit, 3-level digitizer. The output signal coding is as described in Table 2.

Table 2. Output signal coding

	V_{S1}	V_{S2}
$V_e > V_{ref1}$	1	1
$V_{ref2} < V_e < V_{ref1}$	0	1
$V_e < V_{ref2}$	0	0

E. Output buffer

The output buffer (Fig. 7) is designed to transmit data outside the chip through the bond pad, the bonding wire and the 50 Ω off-chip load without deterioration of the data.

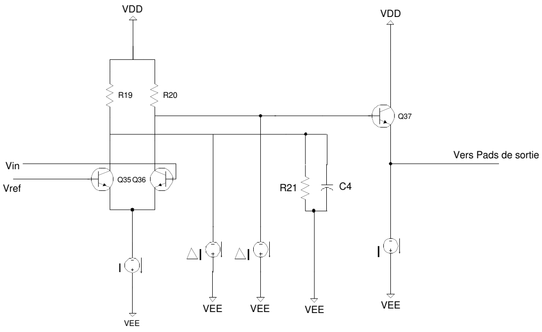

Fig. 7. Schematic of the output buffer

The output voltage provides SCFL (Source Coupled Field Logic) single ended logic levels (0 V / –0.9 V) to be consistent with the Test Auto-correlator designed for ADC high dynamic range tests (see [1]). This output voltage swing is fixed by the resistors R_{19}, R_{20} and the current source I ; the mean value is fixed by the current source ΔI. The output buffer has a high current consumption in order to drive the 50 Ω load with roughly 1 V voltage swing.

Figure 8 shows the microphotography of the chip. Due to the high number of supply pads, for each building block the circuit is 'pad limited'. Hence, a large amount of silicon is filled with decoupling capacitors.

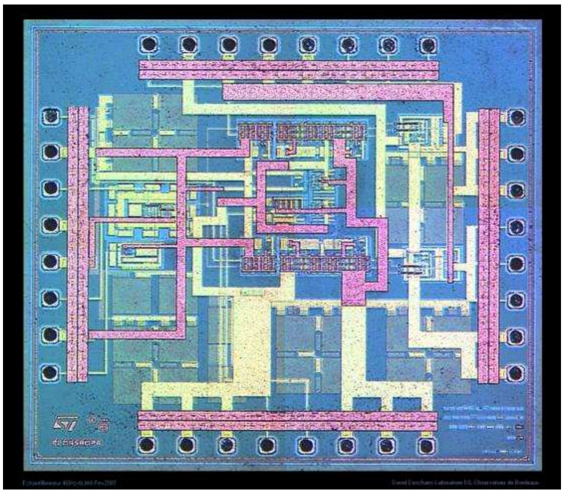

Fig. 8. Microphotography of the chip (February 2001 design)

4. 3, August 2001 design (0.35 µm process)

In this new design the biasing circuits have been changed and improved. The clock amplifier performances have been enhanced and the input adapter amplifier has a better broadband matching. A new package has been chosen; it is well suited to high frequency applications and dissipates more efficiently the heat of the die.

A. Input adapter amplifier

The input adapter amplifier consists of a broadband matched differential amplifier followed by a cascode pseudo-differential amplifier (Fig. 9).

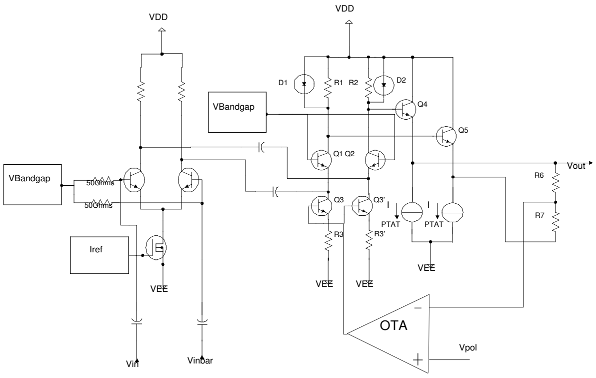

Fig. 9. Schematic of the input adapter amplifier

The current sources of the pseudo-differential amplifier are driven by an OTA. This common mode feedback loop allows us to lock the mean value of the amplifier output voltage to

–150 mV as in the first design. Broadband impedance matching is achieved by on-chip poly-silicon 50 Ω resistors.

B. Clock distributor circuit

We need to transform a 0 dBm 4 GHz sinusoidal waveform into a square signal. The input and the output buffers of the clock amplifier (Fig. 10) are slightly different compared to the February 2001 design. The input stage consists of a LC filter to tune the matching impedance to 4GHz. The output buffers have been modified to improve the clock signal waveforms.

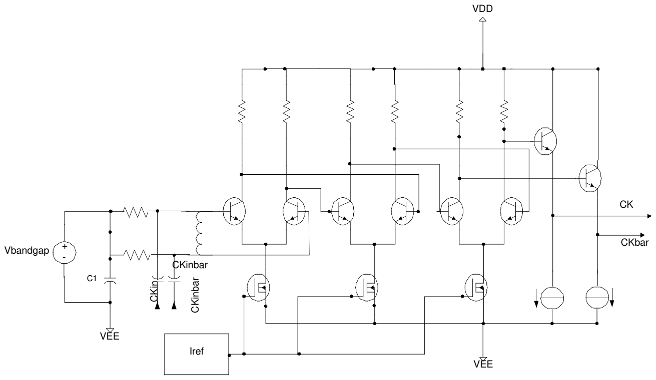

Fig. 10. Schematic of clock amplifier

Figure 11 shows the microphotography of the die. Due to the high number of supply pads for each building block, the die size is pad limited. To minimize the supply voltage ripple, free areas on the chip are filled with decoupling capacitors.

Fig. 11. Microphotography of the chip (August 2001 design)

5. Experimental Results

5.1 Tests of February 2001 design

Our first 2-bit ADC was tested on a 4-layer Printed Circuit Board (see Fig. 5 in [1]). The die was mounted in a 32-pin TQFP package.

Different types of dynamic tests can be made to determine whether an ADC design is suitable for operation (e.g. signal-to-noise and distortion ratio measurements). However, such tests are not decisive in radio astronomy applications for which the input signal is a weak Gaussian statistics noise buried in another white noise signal. In radio astronomy, the conversion efficiency of a weak analog input noise signal can be estimated after a long integration time in a digital auto-correlation system; such a system will be used to qualify our digitizer designs as described in [1].

Our measurements have been made with the test bench shown in Fig. 12. The signal and clock synthesizers (HPE4433B and HP83712B, respectively), and the digitizing oscilloscope (HP54750A) used to analyze the digitizer outputs were all synchronized to a common 10 MHz line. The sampling frequency was 4 GHz.

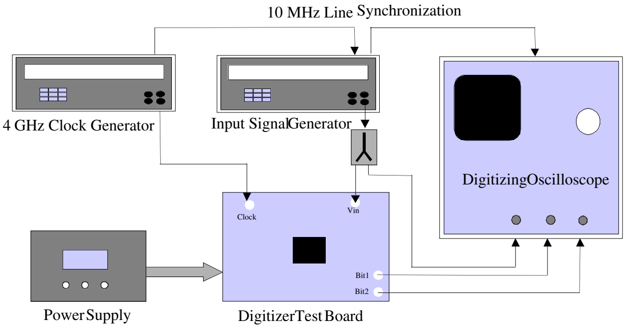

Fig. 12. Two-bit digitizer test bench

The measured hysteresis was about 60 mV (see explanations at the end of this Section). Figure 13 shows the response of the comparators to a 3 GHz sinusoidal input signal (upper plot; the amplitude level is –12 dBm). The lower plots show the 1 GHz output signals on the 50 Ω off-chip load. The output voltage swing is 850 mV. The rise and fall times of the output signal loaded with a 50 Ω impedance are about 130 ps (dV/dt = 6.5 mV/ps). The chip dissipates 652 mW and the die area is roughly 5.4 mm^2. The rejection ratios between the 4 GHz 0 dBm input clock signal and the comparator input and the chip output were measured to be –29 dB and –27 dB, respectively.

Our measurements have shown that the comparison and sampling functions are performed well for clock rates up to 4.9 GHz.

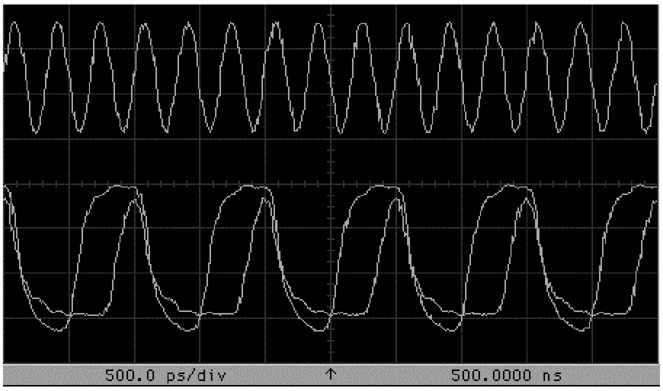

Fig. 13. Measured output waveforms (lower plots) in response to a 3 GHz input signal (upper plot); the digitizer clock is at 4 GHz

The measured –0.5 dB bandwidth of the input amplifier goes up to 4.4 GHz and the –3 dB bandwidth is 2 to 9.8 GHz while the amplifier gain is roughly 12 dB. Table 3 summarizes some main characteristics and results for this first 2-bit digitizer.

Table 3. Characteristics of our first 2-bit digitizer

Voltage supply	±1.25 V
Sampling frequency	4 GHz
Max sampling rate	4.9 GHz
-0.5 dB bandwidth	2-4.4 GHz
Hysteresis	60 mV
Output signal voltage swing	850 mV
Current consumption	260 mA
Die area	5.4 mm^2

We have noticed that the digitizer outputs isolation must be improved. This critically depends on the output buffers and output pads in the layout and was corrected in our design of August 2001. The measured hysteresis is not the internal hysteresis of the comparators. There is an important ripple on the reference voltage of about 60 mV. This input of the comparator must be filtered to strongly reduce the ripple mainly due to the clock signal.

5.2 Tests of August 2001 design

This digitizer has been tested on a 4-layer Printed Circuit Board (Fig. 14). The upper layer is dedicated to the analog input, clock signals, and the output logic signals, and distributes part of the positive power supply. The second layer is a ground layer to form a microstrip circuit. The signal paths are matched to 50 Ω. The die is mounted in a 36-pin VFQFPN package. This package is better adapted to RF applications than the previous TQFP package. Our measurements show that the comparison and sampling functions are adequately performed up to 5 GHz. The test bench was similar to that used for our February 2001 design (see Fig. 12).

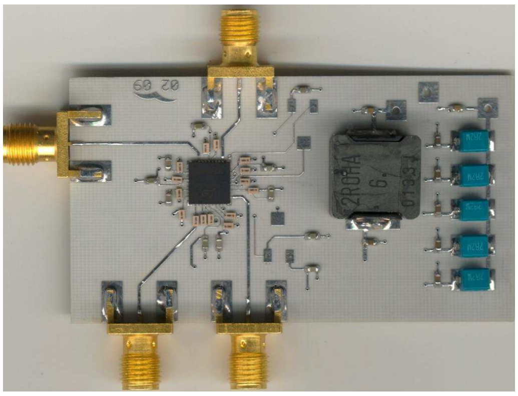

Fig. 14. Test board used for the 2-bit design of August 2001

The measured hysteresis is below 10 mV. Fig. 15 shows the digitizer response to a 3 GHz sinusoidal input signal (upper plot; the amplitude level is –5 dBm). The lower plots show the 1 GHz output signals on the 50 Ω off-chip load. The output voltage swing is 800 mV. The rise and fall times of the output signal are similar to those measured for the February 2001 design. The chip dissipates 975 mW and the die area is 6.5 mm^2. The rejection ratio between the 4 GHz 0 dBm input clock signal and the input adapter amplifier is –30 dB.

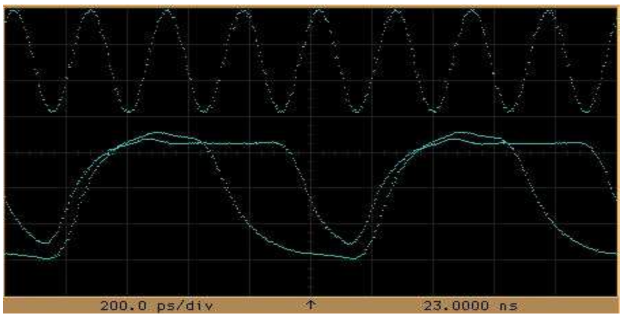

Fig. 15. Measured output waveforms (lower plots) in response to 3 GHz input signal for a 4 GHz sampling clock

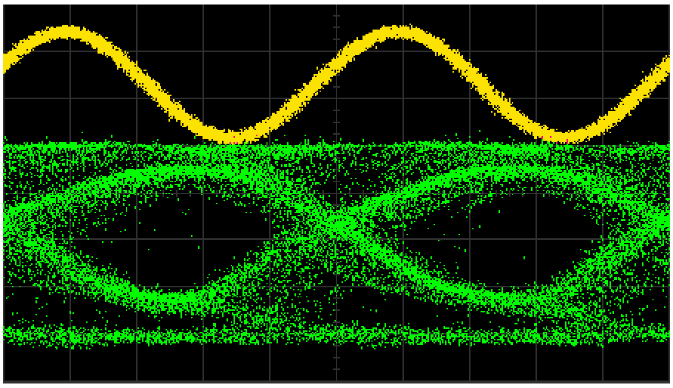

Fig. 16. Eye diagram of digitized output

In Fig. 16 we show the eye diagram for a 2 GHz input signal with 4 GHz sampling clock (upper plot). The amplitude of the open eye is around 600 mV and the horizontal axis corresponds to 50 psec per division.

Our simulations show that for this design the –0.5 dB and –3 dB bandwidths of the input amplifier are 2 to 4.3 GHz and 2 to 9.5 GHz. The amplifier gain is roughly 3.3 dB. Table 4 summarizes some main characteristics and results of this 2-bit digitizer.

Table 4. Characteristics of our 2-bit digitizer design (August 2001)

Voltage supply	±1.25 V
Sampling frequency	4 GHz
Max sampling rate	5 GHz
-3 dB bandwidth	2-9.5 GHz
-0.5 dB bandwidth	2-4.3 GHz
Hysteresis	~ 10 mV
Output signal voltage swing	800 mV
Current consumption	390 mA
Die area	6.5 mm^2

The tests undertaken on this complete 2-bit ADC circuit are satisfactory. In particular, interactions between the two digitizer outputs have been drastically diminished. The filter placed on the reference voltage has greatly decreased the hysteresis level.

7. Conclusion

Two high speed 2-bit SiGe ADCs have been developed using the SiGe BiCMOS 5M1P 0.35 µm process from STMicroelectronics. Details of our designs and first results of dynamic tests have been given. Our measurements show that trade-off between low power consumption and wide bandwidth (2 GHz) is possible and that the ALMA requirements are within reach. The performances of the 2-bit digitizer designed with the BiCMOS7 newer technology (0.25 µm process) will be reported separately as well as the results of our 3-bit designs with 0.25 µm processes.

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