ALMA Memo No. 410

Designing and Prototyping of 2-4 GHz Bandpass SiGe Digitizers and Associated Test Equipment for the *ALMA* Project. I

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Abstract
In this first paper we describe the approach followed to design and experimentally test the high speed and broad band analog-to-digital converters (ADC's or digitizers) required for the *ALMA* project. Our prototypes are based on monolithic digitizers implemented in a BiCMOS 0.35 or 0.25 μm SiGe process with 3 or 8 quantization levels and 4 giga samples per second rate for an input signal from 2 to 4 GHz under full Nyquist condition. We have adopted a conventional flash converter architecture to design three different 2-bit digitizers and one 3-bit digitizer. The experimental results obtained with our first 2-bit digitizer ASIC show that sinusoidal input signals are properly sampled for clock rates up to 4.9 GHz. The design details and high dynamic range tests of our ADC's will be reported in forthcoming papers. A specific digitizer test equipment providing the auto-correlation and spectral analysis of the digitized signal has been developed to characterize our designs and provide the necessary feedback to the ASIC design team. It includes a broad band noise generator, a demultiplexing unit following the digitizer under test, a 16-lag auto-correlator, and FFT and display units. This equipment will also play a major role at the pre-production stage and for qualification/acceptance at the production stage. We suggest that the demultiplexing scheme developed for the digitizer test equipment could be used as a basis for multi-bit synchronization of the demultiplexed signal in front of the *ALMA* fiber optic transmitter system.

1. Introduction

The rapid evolution of integrated circuit technologies tends to favour digitization of broad bandwidths early in the processing stages of the radio astronomy signal. This trend, not only increases the sensitivity performances or the amount of processed information, but also facilitates the replication of digital sub-systems in large arrays of radio antennas, thus improving the reliability of complex arrays. Continuous digitization of the incoming signal is performed at critical points of the radio processing chain, the analog-to-digital converters (ADC's or digitizers), from which all signal samples are collected and coded in synchronism throughout the array. Together with other digital circuitry (astronomical delay compensation and signal cross-correlation) they allow the astronomers to achieve the flexibility and high dynamic range required in spectroscopic observations. ADC's and digital cross-correlators are thus key elements to multi-narrow band (spectroscopy) and continuum high precision measurements of the radio source visibilities.

This paper is the first of a series of papers describing: *(i)* our first 2-bit and 3-bit ADC designs and laboratory tests on printed circuit boards, *(ii)* proposed solutions for fast demultiplexing behind the ADC in front of the fiber optic transmitter system and, *(iii)* the main characteristics of a test equipment including a noise source and test bench dedicated to high dynamic range tests of our prototype and pre-production samplers.

In Section 2, we first comment some performance specifications and briefly describe the system context relevant to the *ALMA* digitizers. In Section 3, the adopted ADC technology and circuit architecture are described in general terms. In Section 4, we give details on some experimental tests made with our first 2-bit sampler. In Section 5, solutions to the design of the multi-bit demultiplexing module required after the ADC are briefly discussed. Finally, in Section 6, the main features of the digitizer test equipment are presented. (An intermediate progress report was published in [1]. Detailed reports on the designs of our ADC's are given in [10].)

2. Specifications and System Context

Each one of the 64 antennas of the *ALMA* array comprises 8 ADC's (4 per polarization) each digitizing 2 GHz IF bandwidth. Top level specifications are summarized in Table 1.

We first note that designing the *ALMA* high speed digitizers (4 GHz clock) implies to have access to high speed integrated circuit technologies (SiGe, GaAs or InP) and that bandpass sampling requires to buffer, amplify and digitize frequencies up to 4 GHz and in fact well above this limit for proper operation.

Designing highly stable and 'spectrally clean' 3-bit digitizers is a significant achievement compared to the usual 2-bit, 3- or 4-level case because signal detection in radio astronomy observations requires long time integrations of continuous input signals. The net result compared to two bits is a higher figure of merit (see below), a 6 dB gain in signal-to-noise ratio (assuming ideal ADC's with quantization noise only), and better protection against radio frequency interferences. We further note that with 8-quantization levels, matching of the comparator thresholds, and minimization of timing mismatches (and thus of encoding errors), are a difficult design goal.

Table 1. *ALMA* digitizer performance specifications

Input BW	**2-4 GHz**
Sample clock	**4 GHz (250 ps)**
Bit resolution	**3 bits** (and 2 bits)
Quantization levels	**8**
Aperture time	**≤ 50 ps**
Aperture Jitter	**~ 2 ps**
Small indecision level	**~ a few mV**
Low power dissipation	**< 2 W** (sampler chip)
Output demultiplexing factor	**1/16**
4 GHz clock distribution	**PLL**
Fine delay command	**≤ 1/32th of one sample**

The aperture time, or the average period of time required to sample the signal, is related in part to the finite rise time of the sampling clock and must be kept small. The attenuation due to finite aperture time varies as $\sin(\pi u)/(\pi u)$ and reaches -0.58 dB at 4 GHz for 50 ps aperture time. The -0.44 dB roll-off from 2 to 4 GHz implies little degradation of interferometer sensitivity [2], and is well consistent with the maximum ripple accepted at the downconverter output level.

The aperture jitter, or variation in the times at which the sampling process occurs, is related to phase errors in the sampling clock signal. It limits the effective signal-to-noise ratio and should remain around 2 ps with a 4 GHz clock. We thus need highly stable (PLL) clock generation and good immunity to temperature drifts and interferences.

The comparator indecision level (hysteresis) should be small and around a few mV. In our design this level corresponds to a small fraction of the input r.m.s. voltage. The digitizer threshold voltages are thus slightly influenced by the input signal voltage variations.

Our initial and updated surveys of many Web sites presenting commercial Flash ADC's and Track/Hold amplifiers with conversion rates above one giga sample per second (Gs/s) show that the product required for *ALMA* is not available [3]. Some devices work around 1 to 2 Gs/s, and one goes up to 4 Gs/s. However, there is no digitizer with an input bandwidth up to 4 GHz. In addition, commercial ADC's offer more bits than actually required for radio astronomy applications and their high power dissipations ~ 3 to 8 W is thus not well suited to the *ALMA* project; our goal here is less than 2 W for 3 bits. The fastest commercial Flash ADC's or Track/Hold amplifiers use bipolar Silicon or GaAs technologies. We note that InP seems less competitive in terms of cost and access.

The digitizer performances can be estimated and compared by means of a universal figure of merit. Following [4], this figure of merit is defined by

$$M = 2^N F / P_d$$

where N is the effective number of bits, F the maximum frequency at which Nyquist sampling is still possible, and P_d the power dissipation. With our designs N = 3 and we expect F = 5 GHz (or more) and P_d < 2 W giving M > 20 GHz/W whereas the operational and most elaborate digitizers available in radio observatories have M ≈ 2 GHz/W.

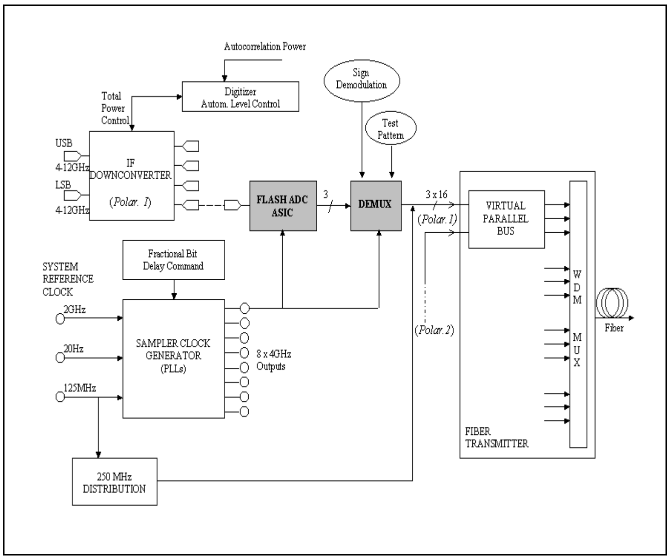

Fig. 1. *ALMA* digitizer in the system context

The demultiplexing stage which follows the sampling stage is necessary for adequate interfacing to the *ALMA* fiber optic transmitter (Fig. 1), and to lower the three continuous 4 Gs/s data rates delivered by each digitizer to adequate bit rates for signal correlation. We have adopted a design in which we separate the sampling/quantization function from the demultiplexing function. This should minimize any potential coupling of the digital outputs with the analog input and thus improve the signal-to-noise ratio and dynamic range of the digital conversion stage. This design choice is reflected in Fig. 1 (the 'Flash ADC' and 'DEMUX' are not implemented in the same ASIC). Fig. 1 also shows important *ALMA* system context functions. In particular, we show the digitizer clock distribution and suggest re-synchronization of the DEMUX output data to the 125 MHz system clock. There are four ADC pairs and demultiplexing units for the two IF downconverters in each antenna of the array (Polar 1 and 2 in Fig. 1).

The sampler clock generator produces and distributes a 4 GHz sine wave to each of eight sampler modules per antenna. The phase of this sine wave can be steered by steps of 11 degrees in order to compensate for the fine part of the astronomical delay. This is performed by a DDS chip, under the control of real-time software. An accurate PLL translates its output to 4 GHz (see also http://iram.fr/TA/backend/samclock).

3. *ALMA* Digitizer

Our team develops both 2-bit and 3-bit SiGe digitizers. Our 2-bit design can be seen as the *ALMA* fall-back solution for interim array operation.

3.1 Adopted technology

The III-V (GaAs or InP) technology is often used for operation at the high frequencies required for *ALMA* [see e.g. 5]. Usually, classical technologies based on Silicon are not fast enough to work at sample rates beyond 1 to 2 Gs/s [6], [7]. However, technologies based on SiGe heterojunction bipolar transistors (HBT) are competitive with III-V technologies in the 1 to 10 GHz range [8]. In addition, SiGe tends to become a low cost Silicon process competing with more expensive high performance GaAs processes.

Our designs are based on the SiGe BiCMOS 0.35 µm and 0.25 µm processes from STMicroelectronics. They include CMOS transistors and SiGe bipolar transistors with 45 GHz and 75 GHz transition frequencies for the 6 G and 7 processes, respectively. These processes allow us to design very high-speed building blocks to achieve broad bandwidth amplifier and comparator cells without excessive amounts of power. The power supply is limited to 2.5 V while most ADC's are designed and optimized for higher voltages. The power supply is often 5 V in GaAs technologies [5], whereas it does not exceed 3 V in Si-SiGe technologies [7]. Our digitizer designs are thus optimized for low voltages and low power consumption.

3.2 Adopted design

Flash ADC's are well suited to the conversion of broad band signals and to high frequency operation. As they use simultaneously $2^N - 1$ comparators for an N-bit conversion process, every bit resolution quickly increases the size and cost of the ADC core circuitry. Hence, Flash ADC's available on the market are limited to about 8 bits. This is more than required for radio astronomy applications in which 3-bit operation already improves the traditional 2-bit case (see Section 2). In Flash ADC's, quantization of the input signal is performed before sampling by comparing with reference thresholds; the sampling function stage is thus, at first order, less critical, and is physically implemented in latches. We have adopted this design for the *ALMA* 3-bit and 2-bit digitizers (Fig. 2).

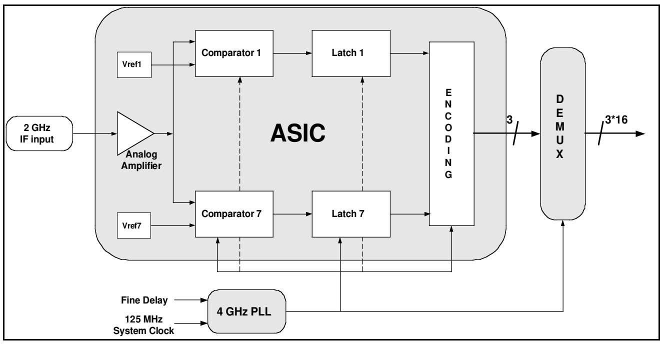

Fig. 2. *ALMA* digitizer block diagram

The ASIC chip integrates an input adapter amplifier, comparators followed by latches, an encoding circuit, and output buffers. The 2 GHz wide input signal is amplified and compared with high and low thresholds (V_{ref1} to V_{ref7} in Fig. 2). The chip layout requires special care in order to minimize errors due to routing path mismatches between the input adapter amplifier and the comparators as well as between the clock distribution module and the comparators. (The demultiplexer, with internally generated 250 MHz, is described in Section 5.)

3.3 Digitizer overview & First designs

The 2-4 GHz input analog signal delivered from one of the four outputs of the IF down-converter module (Fig. 1) is a white noise signal with Gaussian statistics. The first element of the digitizer ASIC is an analog amplifier (Fig. 2) which converts the asymmetrical input signal into a differential one. Its input is matched to 50 Ω. The frequency response of this amplifier must be linear and the ripple over 2-4 GHz within ± 0.5 dB. The digitizer input level is controlled in the IF downconverter with ± 0.25 dB attenuator steps placed in the output paths of each IF down-converter. Sampling is performed in the comparators each one including one comparator and two latches operated in a master-slave configuration and clocked at 4 GHz (Fig. 3). This structure suppresses metastability state by providing more amplification of the input signal and better conversion speed by holding a stable comparison result. The 4 GHz clock signal is equally distributed to 7 comparators (or to 2 comparators in the 2-bit design). The thresholds comprise a zero reference voltage and are set around ± 0.5 σ, 1 σ and 1.5 σ where σ is the r.m.s. voltage at the common input of the comparators. These levels are well above the indecision region and below the comparator supply voltage; they are kept constant and their exact values will be tuned with an accurate division voltage chain to minimize the quantization losses.

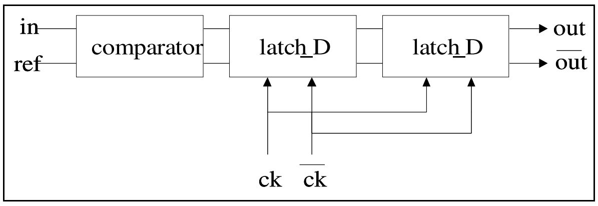

Fig. 3. Sampling cell topology

The digitizer encoding is not yet finally adopted. It is related to the look-up tables of the digital FIR filters which translate between the digitizer code and the 4-level correlator chip code of the *ALMA* Baseline Correlator. The encoding should minimize the power consumption and minimize errors with minimum bit changes. It should also permit easy identification of the signal sign (Sign Demodulation in Fig. 1). The adopted coding outputs for our 2- and 3-bit designs are shown in Table 2.

Table 2. Three- and Eight-level coding outputs

	V_{S12}	V_{S22}
$V_e > V_{ref1}$	1	1
$V_{ref2} < V_e < V_{ref1}$	0	1
$V_e < V_{ref2}$	0	0

V_{input}	D_2	D_1	D_0
$V_{in} < V_{ref0}$	0	0	0
$V_{ref0} < V_{in} < V_{ref1}$	0	0	1
$V_{ref1} < V_{in} < V_{ref2}$	0	1	1
$V_{ref2} < V_{in} < V_{ref3}$	0	1	0
$V_{ref3} < V_{in} < V_{ref4}$	1	1	0
$V_{ref4} < V_{in} < V_{ref5}$	1	1	1
$V_{ref5} < V_{in} < V_{ref6}$	1	0	1
$V_{in} > V_{ref6}$	1	0	0

We deliver SCFL (Source Coupled Field Logic) single ended logic levels (0 V/-0.9 V) for compatibility with the digitizer test equipment. However, for the *ALMA* system smaller voltage swing is preferable (e.g. 0.4 V swing with standard Current Mode Logic, CML).

Table 3 summarizes the ASIC designs performed in the year 2001. There are two 6G 2-bit designs; the 2001 August design is more 'robust' in terms of technological dispersions and contains new clock amplifiers. The 2-bit BiCMOS 7 ASIC design of December required implementation of new tools and corresponds to an important and robust technology evolution. This 2-bit digitizer can be considered as our fall-back solution for interim *ALMA* operation. Our first 3-bit design of May, 2001 will evolve after full performance testing into a BiCMOS 7 design.

Table 3. First prototype *ALMA* digitizers with 0.35 and 0.25 μm SiGe processes from STMicroelectronics

	Foundry Run Date	***Packaging***
2-bit BiCMOS 6G *(0.35 μm)*	February, 2001	TQFP32
3-bit BiCMOS 6G *(0.35 μm)*	May, 2001	VFQFPN44
2-bit BiCMOS 6G *(0.35 μm)*	August, 2001	VFQFPN36
2-bit BiCMOS 7 *(0.25 μm)*	December, 2001	T.B.D.

3.4 Track/Hold and Flash ADC configuration

The alternative to the quantization/sampling approach adopted in our design is : *(i)* sampling the input signal first by means of a Sample/Hold (or Track/Hold) circuit and, *(ii)* implementing quantization in a following stage. This could facilitate the quantization process and perhaps help better meeting some of the *ALMA* specifications although there is no experience at the high frequencies required here for a Track/Hold in front of an ADC. To this end, a GaAs sampler has been designed at the Arcetri Observatory and the University of Florence for the *ALMA* system [9]; it could be used with our Flash ADC in a specific multi-chip package.

4. First SiGe, 2-bit Design: Simulations and Results

The design details for all circuits mentioned in Table 3 are given in [10]. In this Section we concentrate on simulations and results obtained with our first SiGe 2-bit design of February, 2001. The ASIC generic configuration is that given in Fig. 2 with two comparators and two reference voltages. The die is mounted in a 32-pin TQFP package. (This packaging was not optimized for high RF operation.) The chip is shown in Fig. 4 and dissipates 650 mW with a symmetrical ± 1.25 V; its size is 5.4 mm^2. Due to the high number of supply pads for each building block the circuit is ‘pad limited’. Hence, a large amount of die area is filled with decoupling capacitors.

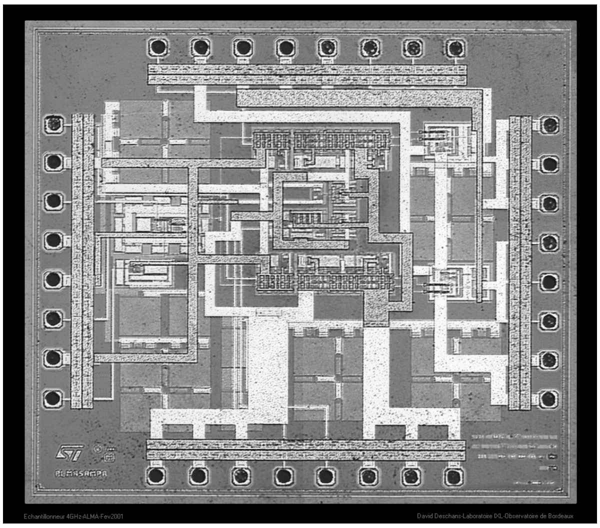

Fig. 4. Microphotograph of our first SiGe, 2-bit digitizer ASIC

All of our simulations were made with Cadence CAD tools. They take into account the extracted view of the design which includes all parasitic capacitors and resistors. In addition, the inputs and the outputs include the parasitic elements of the bond pads, the bonding wires, the lead frame and the package. The simulated -0.5 dB bandwidth of the input amplifier goes up to 4.4 GHz and the -3 dB bandwidth is 9.8 GHz. The amplifier gain is 12.2 dB.

Our comparator design has been tested in the laboratory on a 4-layer Printed Circuit Board shown in Fig. 5. The upper layer carries the analog input and clock signals and distributes the power supply. The second and fourth layers are ground layers. The third layer carries the output logic signals.

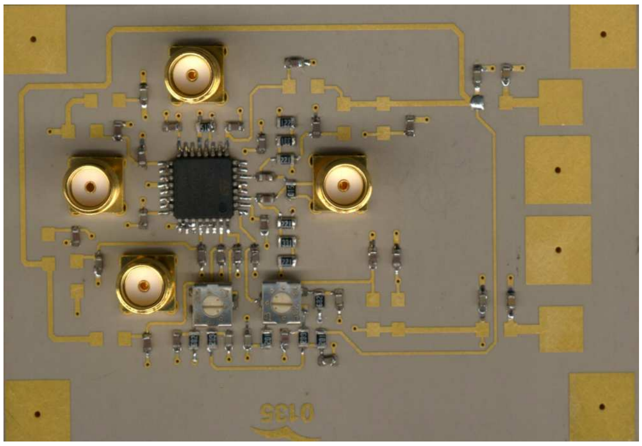

Fig. 5. Printed circuit board and 2-bit comparator ASIC used for laboratory tests

Our measurements show that the comparison and sampling functions are correctly performed for clock rates up to 4.9 GHz. In these measurements, the signal and clock synthesizers and the digitizing oscilloscope (HP 54750A) used to analyze the output signals are all synchronized to a common 10 MHz line. In Fig. 6 we show the response (lower plots) to a 3 GHz input signal (upper plot). The amplitude of the input signal is -12 dBm and the output signals are on the 50 Ω off-chip load. The output frequency is 1 GHz as expected with 4 GHz clock; the output voltage swing is 850 mV.

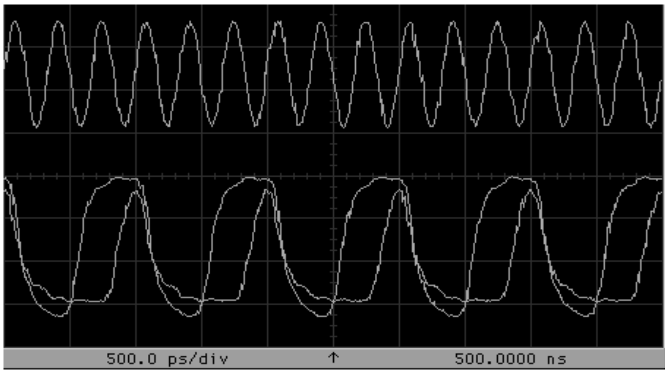

Fig. 6. Measured output waveform (lower plots) in response to 3 GHz input signal (upper plot) and 4 GHz clock

The measured rise and fall times of the output signal loaded with a 50 Ω impedance are around 130 ps. The measured rejection ratios between the 4 GHz +0dBm input clock signal and the comparator input on one hand, and chip outputs on the other hand are -29 and -27 dB, respectively.

It is interesting to note that the ratio *d*V/*d*t, where *d*V is the output voltage swing, is an important parameter to characterize the circuit performances. With dt = 130 ps (our measurement) and SCFL logic used here (dV = 900 mV) we obtain dV/dt = 7 mV/ps, while with standard CML (dV = 400 mV) we expect a rise time well below 100 ps for the same design.

5. *ALMA* Digitizer Demultiplexing Unit

Various solutions are being investigated to process the Flash ADC output data rate before transmission (see Fig. 1) to the Fiber Optic System link. The sampler ASIC output is connected to a Fast Demultiplexing Unit (FDU, or DEMUX box in Fig. 1) in front of the Virtual Parallel Bus (VPB). With 1/16 demultiplexing factor the FDU delivers 16 times 3 bits or 250 Mbits/s in 48 lines to be connected to each VPB of the Fiber Transmitter. This is consistent with the 12 Gbits/s output data flow from each sampler ASIC and with the input rate accepted by each VPB digital serializer and optical combiner implemented in the Fiber Transmitter. The FDU designed for the digitizer test equipment is made up of three single bit demultiplexing boards (Fig. 7, and see following Section). Each board comprises a 1/16 demultiplexer and a synchronizer allowing multi-bit demultiplexing operation. The 1/16 demultiplexer consists of several logic layers, the first one using commercial high speed GaAs IC's. The synchronizer can be seen as a PLL stage detecting whether the (equivalent) 1/16 logic counters of two chained demultiplexers operate in the same phase state or not.

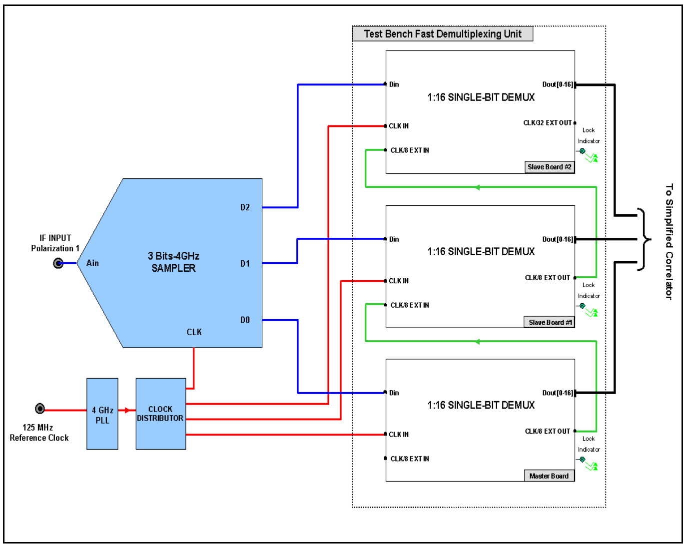

Fig. 7. Fast Demultiplexing Unit (FDU) block diagram for the digitizer test equipment

Designing for the *ALMA* system an upgraded version of the FDU associated to the digitizer test bench poses a significant problem due to the necessary long-term reliability expected for such an equipment in comparison with a board operated in the laboratory environment. Moreover, a proper design has to take into account easiness of production and test (i.e minimization of board adjustments).

At the moment, no commercial demultiplexer allows us to phase 3 bit signals at high rates. Three main possibilities are thus considered:

a) Synchronization of three single-bit commercial demultiplexers using the technique implemented in the digitizer test equipment;
b) Use of commercial high speed gate arrays, if available;
c) Development of a specific 3-bit demultiplexing ASIC.

Option *b)* would require careful investigation while option *c)* could not be cost efficient but is worth investigating. Option *a)* has been successfully tested (see [11]). Nevertheless, the number of demultiplexing units to be synchronized being now fixed to three, a second generation design has to be developed using updated commercial off-the-shelf technology in order to offer a more compact size, less power consumption and a well-known electrical interface.

6. *ALMA* Digitizer Test Equipment

The digitizer test equipment under development will provide high dynamic range characterization of the sampler ASIC and, therefore, necessary feedback to the ASIC design team all along the different foundry runs (see also http://iram.fr/TA/backend/simplcorr). In addition, we propose to use the digitizer test bench and associated equipment for characterization and quality tests at the production stage.

6.1 Overview

The tests performed with the digitizer test equipment are:

a) Actual statistical distribution of the signal samples. Thresholds from each of the 2 or 7 comparators will be extracted and compared to their nominal values;
b) Time stability. The autocorrelation sequence zero lag is an 'image' of the signal power whose stability over long periods of time is of prime importance, and can be estimated by means of the input samples Allan variance;
c) ASIC input frequency response. The input signal being a white noise, the Fast Fourier Transform (FFT) of the auto-correlation function should be flat. In practice, one will obtain a response including ripple within the passband (due to input buffer mismatch for instance). The FFT spectrum will give the frequency response of the ASIC analog input stage and will underline any frequency distortion.

The physical architecture of the digitizer test equipment is shown in Fig. 8. It comprises both commercial instruments (clock generator, power splitter, power supply, plug-in data acquisition board, PC) and home made units (noise source, fast demultiplexing unit, simplified correlator board).

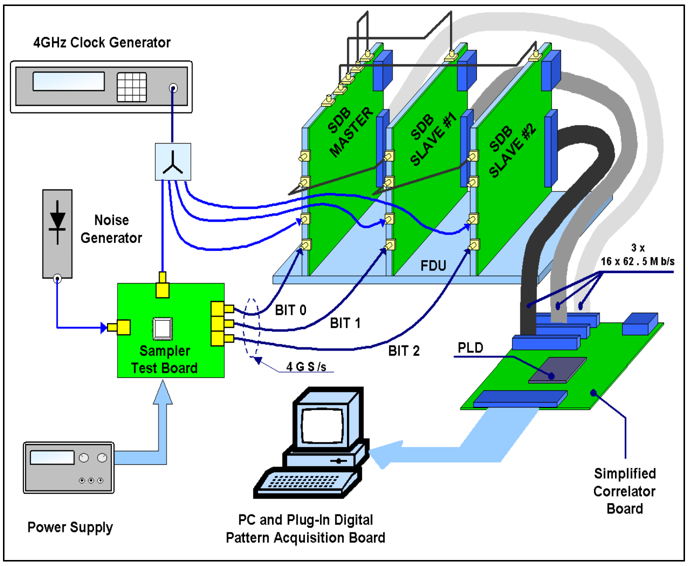

Fig. 8. Physical architecture of the digitizer test board and associated equipment

The noise source is flat over the input frequency range within ±2 dB and is able to deliver up to +23 dBm over 2 GHz bandwidth. The sampler ASIC is powered thanks to an adjustable power supply to allow stability measurements versus supply voltage.

The number of auto-correlation lags is set to 16 which represents a good compromise between complexity and performance. Thus, the FDU acquires a set of 16 consecutive samples at a rate of 4 Gs/s. Once the samples have been captured, they are distributed at a lower rate to be processed off-line by the simplified correlator board.

The simplified correlator board (SCB) computes the auto-correlation function as well as the probability density function of the input samples acquired over a fixed integration time slice. Once this time slice is over, the computed data are transmitted to a plug-in digital pattern acquisition board which sends them over the PCI bus of a computer. The latter supports the test software which computes the Van Vleck correction then the FFT and displays the results (LabVIEW environment). In order to monitor and analyze the effect of different types of physical changes (on-board adjustment, temperature step, etc.), the FFT result will be displayed every second.

6.2 Hardware implementation

Acquisition of the samples and their processing are performed by the FDU and the SCB respectively (Fig. 9). Following an acquisition request from the SCB, the 16-sample packet is parallely transmitted to the SCB. This asynchronous transmission between the FDU and SCB allows us to run the FDU at a sampling frequency independent of the SCB processing speed. During preliminary debugging tests, this feature will allow us to run any sampler chip whichever maximum speed operation is achieved or used.

Because of ultra-high frequencies involved in the FDU and because of sampler bit resolution uncertainty at the time where we have started the test equipment design, a one board per bit architecture has been adopted. A single demultiplexer board is composed of an off-the-shelf GaAs 1/8 demultiplexer as a first layer. Its 500 Mbits/s output rate is down-converted to 62.5 Mbits/s thanks to a second layer made up of a set of two 8-bit registers alternatively latched. This final rate is based on the maximum input rate accepted by the PLD correlator. Once the 16-sample packet has been captured, it is transmitted to the SCB thanks to line buffers.

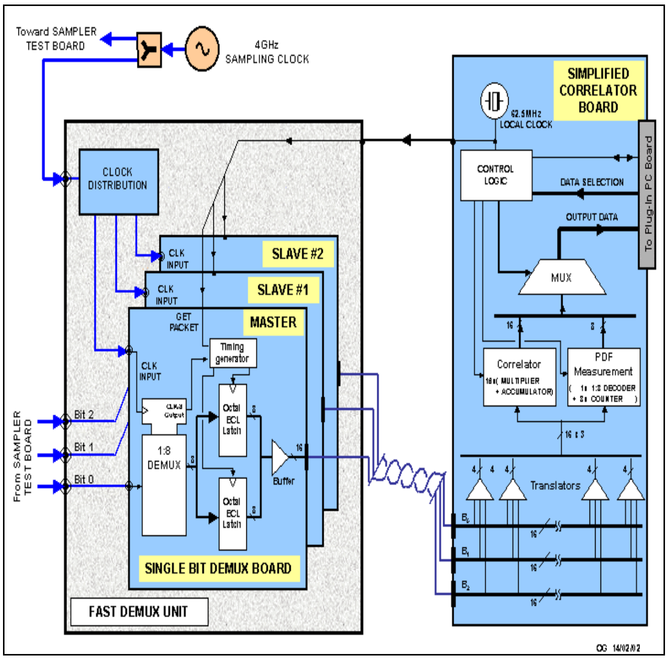

Fig. 9. System block diagram: fast demultiplexing unit (FDU) and correlator board

The auto-correlation and probability density functions are computed within a single programmable logic device (an ALTERA PLD product). The maximum data processing speed is expected to be near 120 Mbits/s.

The noise source (Fig. 8) delivers a white noise over the frequency range 100 MHz to 4 GHz. The output spectral density shape could be either of the lowpass or bandpass type in order to test the sampler ASIC performances in different instrumental configurations. Lowpass and bandpass configurations are selected thanks to an external filter. The output voltage can be adjusted with an internal 1 dB step precision attenuator. The output power stability is optimized thanks to regulated power supplies and by controling the noise source temperature. An OEM temperature controller coupled to the noise source socket provides a constant working temperature.

6.3 Development status

The FDU design is now complete. Tests have shown proper running of the demultiplexing unit beyond 4 GHz sampling clock as well as successful operation of the bit-phasing circuit. The SCB implementation is currently in progress. Computation frequency may go up to 120 MHz according to the PLD timing simulations; this far exceeds the targeted working frequency.

Once all hardware developments will be finished, a data processing software will be implemented using the LabVIEW graphical programming language. Preliminary sampler test results are thus expected to be available soon.

7. Conclusions

Four SiGe high speed digitizers have been designed and fabricated taking advantage of a cooperation with STMicroelectronics. This cooperation allows us to use their foundry and will permit preparation of the highly reliable digitizers required at the *ALMA* production stage.

We have given some details on our first 2-bit design developed with the 0.35 µm BiCMOS 5M1P process from STMicroelectronics. Measurements made on a specific printed circuit board show good agreement with our simulations, and proper signal digitization is observed up to 4.9 GHz clock rate.

Possible schemes have been briefly presented for the multi-bit demultiplexing module required after digitization in front of the Fiber Transmitter of the *ALMA* system. One possibility includes synchronization, as successfully demonstrated with the demultiplexers designed for our digitizer test equipment, of three commercially available single bit demultiplexing chips in a new compact design.

The digitizer test equipment required for qualification and production of the *ALMA* digitizers has been described in general terms. It is nearly completed and will be used to extensively test our 2001 designs, and, at a later stage, to test the pre-production digitizers as well as to qualify the production units.

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