# ALMA memo #383
# A simple technique for disciplining independent demultiplexers

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**2001-07-26**

## 1. Abstract

In every antenna of the ALMA array, the digitizers will deliver 3-bit (or more) samples at the rate of 4 Gigasamples per second. Data is not practical to handle at this speed and needs to be converted to a lower frequency by means of serial-to-parallel conversion. To solve this problem the telecomm industry has developed fast "mux/demux" chips, which unfortunately are single-bit devices. If we use 3 (or more) of them, a synchronization problem arises. The right way of solving this problem would be to design a chip including 3 (or more) demultiplexers on the same die. Should this approach be found not economical for ALMA, this paper describes a method for synchronizing several single-bit commercial demultiplexers.

A prototype circuit including two single-bit devices and synchronization circuitry has been built and successfully tested. The measured timings for acquisition and recovery are presented.

## 2. The synchronization problem

Many manufacturers (Giga, Vitesse, Maxim,Multilink...) now offer IC solutions to the problem of de-serializing the 10Gigabit/sec output flow of a digital optic fiber link. They are intended for the 0C-192 standard which stipulates a 9.952 GHz clock and a 622 MB/s data output. They differ by some features but they all have the same basic structure:

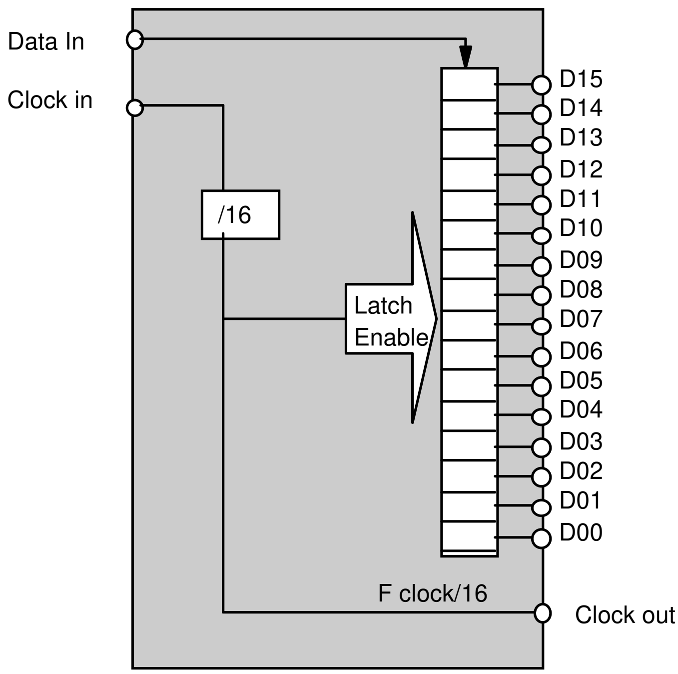


Fig.1 : Generic functional diagram of a commercial demultiplexer

The clock output is generated by division of the fast clock and consequently can have 16 different phases. The phase of the divider is established almost randomly at power-up and in principle it keeps its value indefinitely, provided that the electrical signals are of sufficient quality. For the telecomm people this means that the 16-bit data blocks can have 16 different forms. The state of interest (among the possible 16) is determined by a protocol which sends a sync sequence, and activates a barrel shifter to restore the correct situation. Some lower frequency devices (e.g. the MAX3680) incorporate a pulse swallower that also has the effect of barrel-shifting the data.

For Radio Astronomy we cannot re-use this hardware "as it is", because the sampler delivers 3 (or more) bits with relative significance, which is not the case of the telecomms where the traffic on different OF's are independent. It would also be difficult to find a suitable place to inject a sync sequence, since there is no low-speed stage before the sampler.

**3. The "state locked loop"**

When several demultiplexers are used, their clock outputs need to be forced on the same phase. So will be their data. One can be used as a master and the others just need to be aligned on it. A convenient way to measure the phase difference between two digital outputs is to make use of an XOR gate, followed by an analog integrator. This delivers a DC voltage which is 16-step staircase, where the state of interest (in-phase) has a single determination, corresponding to the maximum voltage. A single comparator can thus determine whether the two outputs are on the same phase or not. If not, an elementary control logic would request to turn the clock off and on for a random number of cycles until the state of interest is acquired. If for any electrical reason the state happens to change, the loop would detect it and go for a new acquisition.

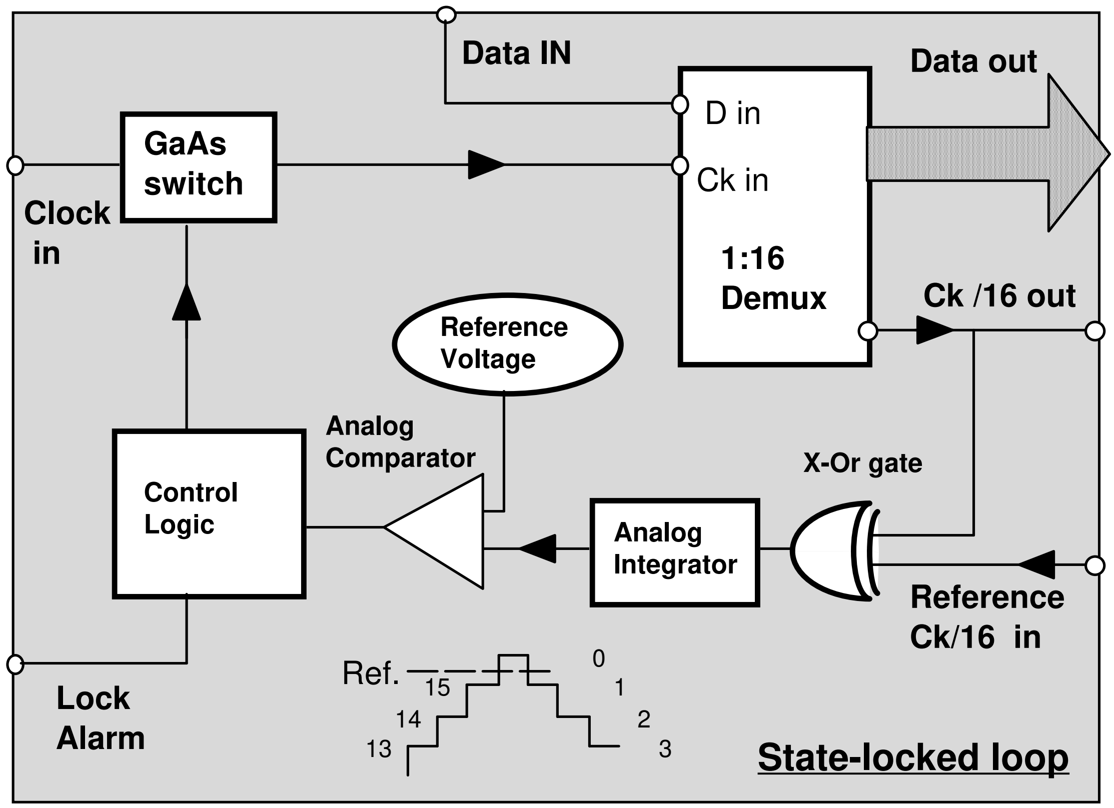


Fig 2. Block diagram of the loop

This circuitry is equivalent to the well known "search oscillator" used in phased locked loops. It differs in the sense that the number of trials necessary to acquire the correct phase is random. Each trial has a 1/16 probability of success. The repetition of trials is a binomial process with a converging-to-1 probability of success, for example 99% is reached after 71 shots. In our case the loop needs to be activated once at power-up and in case of accidental loss of lock. A lock-in time of one second would be fully acceptable. In fact the values that apply make this time much shorter. For multibit operation one demultiplexer is free running and is used as the master for disciplining the others.

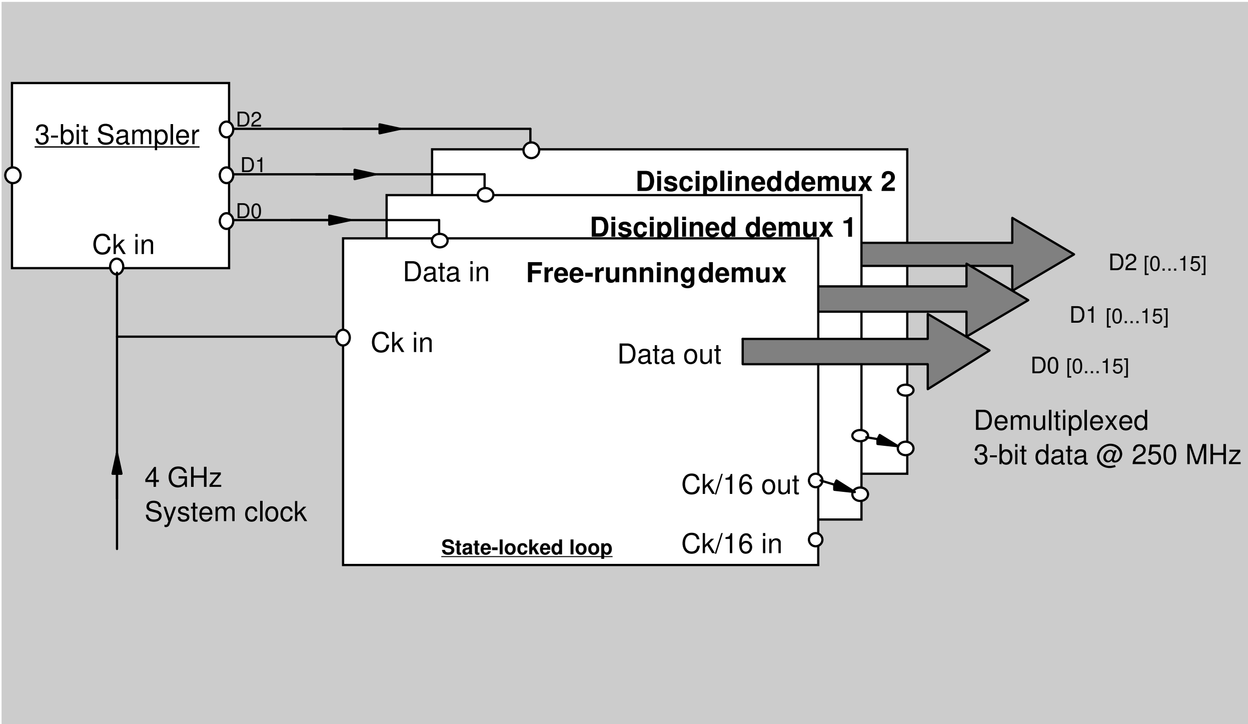


Fig 3. Cascading of loops for multibit operation

## 4. Lab tests

4.1 Hardware description

Two loops operating at 4 GHz have been built and set together. The demux chip is a NEL4616, the GaAs switch is a MGS71008 and the X-Or is an Eclips EL51 operated at 500 MHz. The quasi-analog phase comparator has been tested by applying a few Hz frequency difference between Ref. input and Clock/8, and its output is shown in Fig.4.left. The quality of the sawtooth depends on the shape of the digital signals, which in turn depends on the quality of the implementation. At the board design stage, it is good to apply microwave rules, even if the signals are seemingly digital.

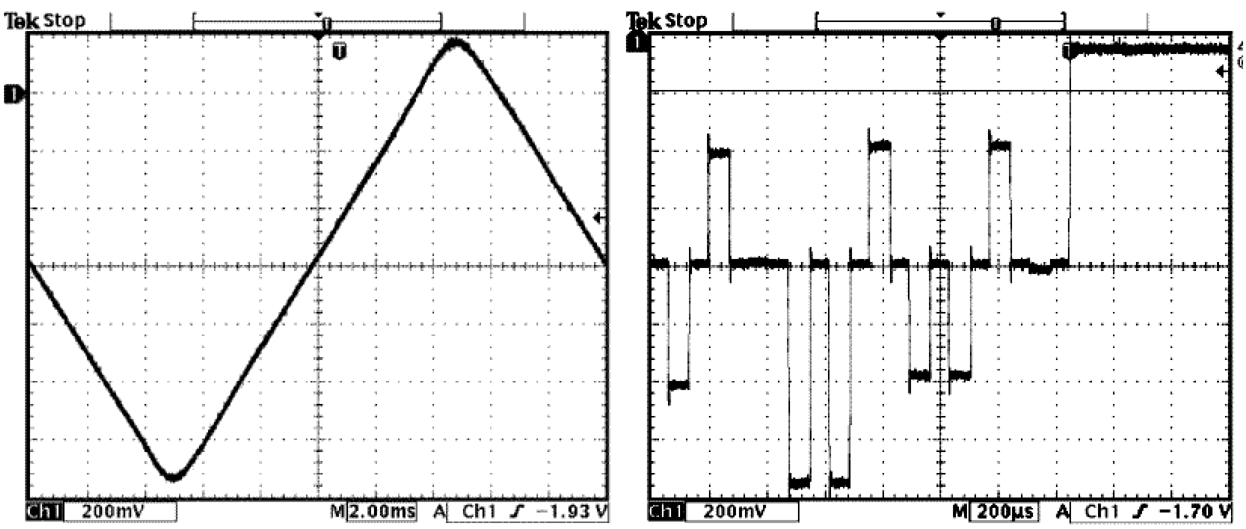


Fig 4. Outputs of the phase comparator Left:static Right:during acquisition

4.2 Lock-in tests

With the same scale, Fig.4 right shows the convergence of a stimulated acquisition sequence. The time constants of the control logic have not been optimized for the fastest possible lock-in, but for safe and stable operation. One can see that a time of 160 microseconds per trial has been practiced. The output of the phase comparator can have 5 different values, and the decision level is shown by an horizontal bar. The central level figures orthogonality, which can be obtained either by quadrature (leading or lagging), or by the clock being stopped. Each trial starts by stopping the clock for a 80-microsecond period. After a few unsuccessful trials, a "good state" condition is detected and the search oscillator is stopped.

We have stimulated repeated acquisition sequences while recording the time needed to get lock. Fig.5 shows the superimposed results of 100 acquisitions. None needed more than 5 milliseconds, which is consistent with probablility theory.

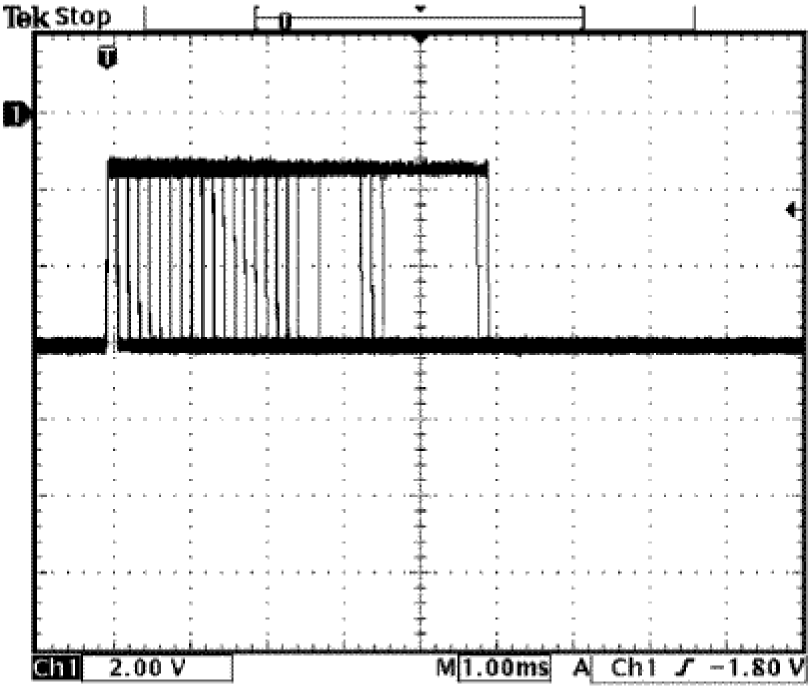


Fig.5: Random time required to get lock, for 100 successive acquisitions.

## 5. Discussion

The loop described above can be seen as a phase-locked loop, where the phase to be followed only has discrete values. It may lock on a false state if the phase comparator output was inaccurate or noisy. In the final application, (with a 1:16 demux), it will have 9 steps (instead of 5 here), but its precision will increase due to a lower operating frequency (250 MHz).

The prototype used here is quite bulky, but with more recent chips, like the Max3950, a design including 4 bits occupying less than 4 square inches of PCB real estate is not unrealistic with current technology. It would have the same functionalities as an especially designed multibit demux IC, but it would be cheaper by a couple of orders of magnitude.

A specialized IC is by far the best issue to the multibit demultiplexing problem. As for now, the telecomm industry, who is market-driven by single-bit applications, is not likely to undergo such a development. Should it be the case for ALMA, the method described above is a possible alternative.