MMA Memo 204:

Digital Filtering in the MMA

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1) Introduction

For the last few weeks we have been investigating the possible use of digital filtering in the MMA baseband/correlator systems. It now looks as if this approach may be practical and can replace all but a single 2-GHz anti-aliasing analog filter in each baseband signal path of the MMA.

2) Design Principle

The fundamental reason that digital filtering at a 4 GHz clock rate is practical for the MMA is that the MMA requires quantization with only 2-bit (2-bit, 4-level sampling is to be used in the MMA). When the words to be filtered in an FIR digital filter are only 2 bits wide, look-up table RAMs can be used for circuit-efficient tap weight multiplication and initial summation. A small RAM with a 256 X 16 configuration can perform tap weight multiplies and first stage summation of 4 samples per clock tick.

Computation of the contents of the look-up table RAMs would be done off-line before an observation, with the multiplication of all possible combinations of 4 samples by their respective 4 tap weights along with the summation of the 4 weighted samples being done using high precision arithmetic. On loading, the results would be rounded to 16 bits to fit into the 16-bit width of the RAMs.

The proposed MMA correlator design contains samplers working from a 4 GHz sample clock. Each sampler will have a de-multiplexed output of 32 X 2 signals at the correlator system clock rate of 125 MHz. To obtain, say, a 128 tap FIR filter, each of the 32 2-bit outputs of a sampler needs to drive a 4-bit shift register. In this configuration, the chip would require 32 of the 256 X 16 RAMs, working at 125 MHz, to handle the full output of a 4-GHz sampler.

As explained in more detail in the next section, such an FIR filter could provide all bandwidths proposed for the MMA (factor of two steps in bandwidth from 31.25 MHz to 2 GHz) while requiring only a single 2-GHz wide analog filter.

3) Implemention

Figure 1 shows a block diagram for a practical FIR digital filter custom chip. The MMA baseband system contains a single 2-GHz wide analog filter as shown. All 32 X 2 outputs (at 125 MHz) from a 4-GHz sampler drives the FIR chip where 32 (times 2) 4-bit shift registers produce a parallel output of 128 consecutive samplers. Thirty-two 256 X 16 look-up table RAMs perform tap weight multiplications and early stages of summation.

An adder tree of 16-bit full adders then sums the output of all 32 RAMs to produce a final digital filter output. Since the correlator chips projected for the MMA will accept only 2-bit wide samples, the 16-bit FIR filter output must be quantized back to the 2-bit format.

The chip shown in Figure 1 works with a 125 MHz clock and produces a single (2-bit) 125 MHz output. If the filter chip is implementing a one half band low-pass (or high-pass) filter on the 4-GHz sampler output, sixteen 2-bit outputs at 125 MHz are required (a factor of 2 decimation from the full bandwidth 32 X 2 sampler output). Thus 16 of the FIR chips shown would be required. With 16 of the chips of Figure 1, a 128-tap one-half band FIR digital filter working at a equivalent clock rate of 4-GHz (with a 2-GHz output) could be effected.

If a one-quarter band FIR filter were desired, only 8 of the FIR chips of figure 1 would be required for a 128-tap filter (they would have different tap weights loaded in the look-up table RAMs). Since there would be 16 FIR chips available, the other 8 chips could be used to provide 128 additional taps resulting in a 256-tap filter. This enhancement in performance is required since, for a given filter performance, roughly twice the number of taps are required as the pass band width is halved.

The result would be that the 16 FIR filter chips could be logically re-wired to supply filtering action with from 128 tap to 4096 tap performance as the desired pass band goes from 2 GHz to 62.5 MHz in bandwidth, thus providing good performance in terms of cut-off slope and out-of-band rejection for all these bandwidths. The 31.25 MHz filter would still have only 4096 taps, and its performance would be thus somewhat degraded; the major implication would be a loss of a little more of the bandpass at the filter edges. However, it is possible that similar degradation would be present in an all-analog filtering system, due to the fact that several filterings and mixings are required to get down to 31.25 MHz.

4) Practical Considerations

The chip described in the last section is not very large as LSI chips go today. The chip requires 32 RAMs with the 256 X 16 configuration and an adder tree of 31 16-bit full-adders. Such a chip would be similar in size to the buyterfly chip NRAO developed for the VLBA correlator. Of more concern that

the size of the chip, however, is its performance. RAMs and 16-bit adders that work at 125 MHz require high performance. A check with a vendor of custom gate array chips, LSI Logic, however, indicates that this performance level in CMOS gate arrays is available.

5) Advantages

A digital filter has the advantages of versatility, stable performance, and probably system-wide cost savings.

The versatility of the digital filter is that, in principle, any filter shape can be generated, subject to the limitations imposed by the number of taps available. For example, a notch filter could be included to knock out an interfering signal; a bandpass filter (rather than low- or high-pass) could place the output band anywhere in the original band at the cost of a less steep cut-off slope; the out-of-band rejection could be improved at the cost of a less steep cut-off slope; and other examples might be conceived. Probably the chief advantage of the digital filter is that it eliminates a large number of analog filters, mixers, and interconnections, all of which may introduce systematic errors into the final results. The output of an FIR filter is flat in phase and does not change with temperature. Furthermore, the bandpass match among different antennas would be much better than with an analog filtering system. There would still be differences due to the front ends, fiber optic IF transmission, and IF conversion to the single 2-GHz-wide IF signal going into the sampler; however, the elimination of all further analog components will certainly improve system performance overall.

Some cost savings may result. In the present design for the baseband converter system, there are 6 analog filters, 2 mixers, 2 (system-wide) fixed local oscillators, and a selector switch, all of which would be eliminated by a digital filter. Since there are 8 basebands per antenna, the number of analog components eliminated is large. These would be replaced by a number of digital boards, but we anticipate that the cost of the FIR chips plus boards plus construction and checkout will be lower than that of an analog system.

One of the important reasons to choose analog IF transmission, rather than< digitizing at the antenna and sending the samples back to the correlator on digital fiber optic channels, is that a large amount of analog machinery would be required at each antenna. If an FIR filter is used, than it may make sense (when the cost of digital transmission drops to the required level) to switch to digital transmission.

6) Disadvantages

The main disadvantage to using a digital filter is that a second stage of 2-bit, 4-level, quantization is required between the analog baseband output and the correlators. Each stage will lower the observational efficiency by a factor of about 0.87 and the combination of two 4-level quantization stages results in an overall efficiency of 0.79, about a 13% loss from a single quantization stage.

One possible way to alleviate this double quatization loss would be to sample with 3-bit, 8-level, samplers. Since the 50% increase in the number of wires would affect only the short interface between the sampler and the filter, this approach would not exacerbate the wiring problem of the correlator very much.

The disadvantage to 3-bit sampling is, of course, the increased cost of the sampler and the increase in the cost of the FIR filter chip itself (the RAMs get larger).

A second way to reduce the double quantization loss would be to offer a 16- level option in the correlators akin to the 9-level option offered by the GBT spectrometer. The FIR filter chip could be made to re-quantize with 16-level precision. This approach would come at the cost of factor of 4 reduction in the number of lags for a given mode. This suggestion is very complicated and requires much more thought to insure its practicality.

7) Computer Simulation

Some work has been done on a computer program to simulate the chip described above. Preliminary simulation results are encouraging and will be presented in a future report. With the simulation effort we should be able to improve our confidence in the digital filter approach. The simulation will also answer the question of how many tap weights are really required to meet the MMA requirements.

The study so far indicates that a 128-tap one-half band filter is probably excessive and either a 64-tap or 92-tap design will be acceptable.

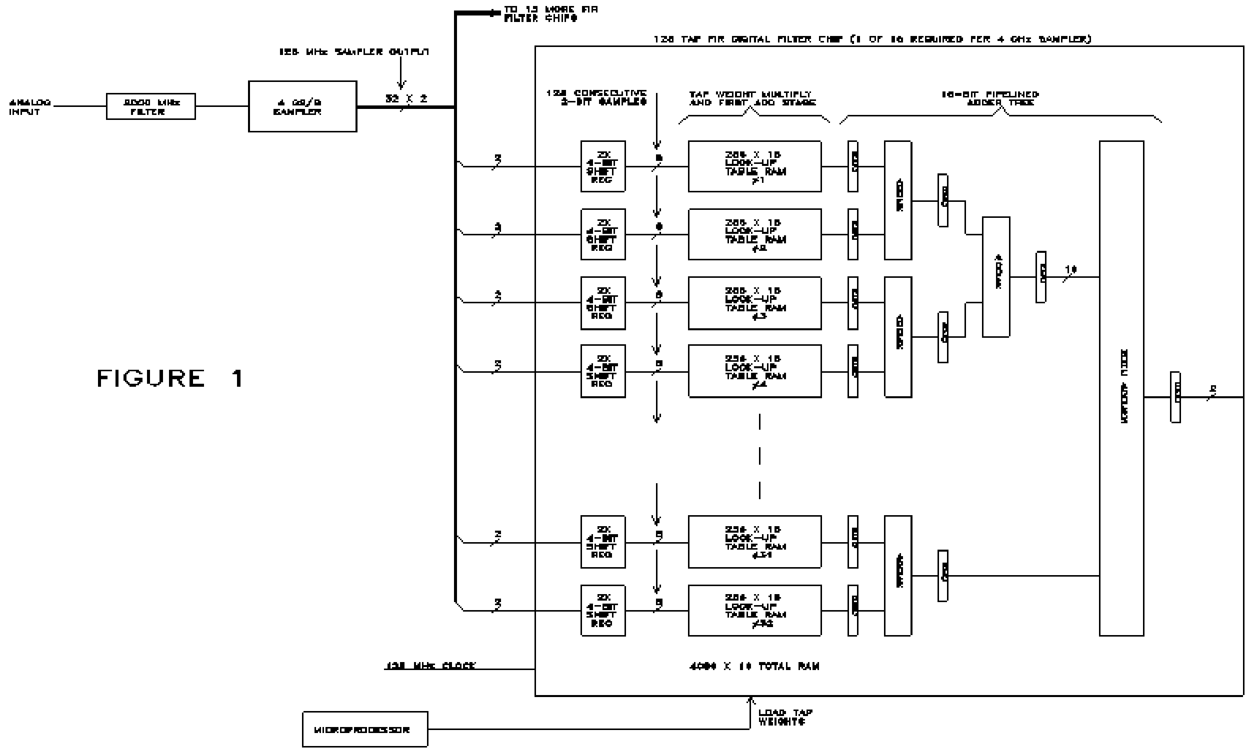
ANALOG INPUT
2000 MHz FILTER
4 GS/S SAMPLER
128 MHz SAMPLER OUTPUT
32 X 2
TO 15 MORE FIR FILTER CHIPS
128 TAP FIR DIGITAL FILTER CHIP (1 OF 16 REQUIRED FOR 4 GHz SAMPLER)
128 CONSECUTIVE 2-BIT SAMPLES
TAP WEIGHT MULTIPLY AND FIRST ADD STAGE
16-BIT PIPELINED ADDER TREE
2X 4-BIT SHIFT REG
256 X 16 LOOK-UP TABLE RAM #1
256 X 16 LOOK-UP TABLE RAM #2
256 X 16 LOOK-UP TABLE RAM #3
256 X 16 LOOK-UP TABLE RAM #4
256 X 16 LOOK-UP TABLE RAM #31
256 X 16 LOOK-UP TABLE RAM #32
128 MHz CLOCK
4096 X 16 TOTAL RAM
MICROPROCESSOR
LOAD TAP WEIGHTS

FIGURE 1